CLAIMS

We claim:

1. A programmable logic device (PLD), comprising a logic core connected to an input/output (I/O) interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein:

at least one PIB can be programmed to perform two or more of:

(a) a double data rate (DDR) input mode in which an incoming DDR data signal is converted into two single data rate (SDR) data signals that are made available to the logic core;

(b) one or more demux input modes in which an incoming data signal is demultiplexed into two or more lower-rate data signals that are made available to the logic core;

(c) one or more DDR demux input modes in which an incoming DDR data signal is converted into four or more lower-rate SDR data signals that are made available to the logic core; and

(d) one or more additional input modes in which an incoming data signal is made available to the logic core without any demultiplexing or DDR-to-SDR conversion; and

the at least one PIB can be programmed to perform two or more of:

(a) a DDR output mode in which two SDR data signals from the logic core are converted into a single outgoing DDR data signal;

(b) one or more mux output modes in which two or more data signals from the logic core are multiplexed into a single, higher-rate, outgoing data signal;

(c) one or more DDR mux output modes in which four or more SDR data signals from the logic core are converted into a single, higher-rate, outgoing DDR data signal; and

(d) one or more additional output modes in which a data signal from the logic core is provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion.

2. The invention of claim 1, wherein the PLD is a field programmable gate array (FPGA).

3. The invention of claim 1, wherein:

the one or more additional input modes comprise a pass-through data input mode and an input register mode; and

the one or more additional output modes comprise a pass-through data output mode and an output register mode.

4. The invention of claim 1, wherein, during each DDR demux input mode:

the incoming DDR data signal is converted into first and second SDR data signals;

the first SDR data signal is demultiplexed into a first set of two or more lower-rate SDR data signals; and

the second SDR data signal is demultiplexed into a second set of two or more lower-rate SDR data signals.

5. The invention of claim 1, wherein, during each DDR mux output mode:

a first set of two or more SDR data signals are multiplexed into a first higher-rate SDR data signal;

a second set of two or more SDR data signals are multiplexed into a second higher-rate SDR data signal; and

the first and second SDR data signals are converted into the outgoing DDR data signal.

6. The invention of claim 1, wherein the PIB supports a plurality of different demux input modes, a plurality of different DDR demux input modes, a plurality of different mux output modes, and a plurality of different DDR mux output modes.

7. The invention of claim 6, wherein:

the plurality of demux input modes includes (1:1), (1:2), and (1:4) levels of demuxing;

the plurality of DDR demux input modes includes (1:1), (1:2), and (1:4) levels of demuxing, each combined with DDR-to-SDR conversion;

the plurality of mux output modes includes (1:1), (2:1), and (4:1) levels of muxing; and

the plurality of DDR mux output modes includes (1:1), (2:1), and (4:1) levels of muxing, each combined with SDR-to-DDR conversion.

8. The invention of claim 1, wherein, to support the input modes, the PIB comprises:

(1) a DDR stage adapted to convert an incoming DDR data signal into two SDR data signals; and

(2) a shift stage and an update stage adapted to demultiplex one or more data signals into two or more lower-rate data signals.

9. The invention of claim 8, wherein:

the DDR stage comprises two flip-flops (FFs), each adapted to receive the incoming DDR data signal and generate a different one of the two SDR data signals;

the shift stage comprises two sets of one or more FFs, each set configured as a shift register; and

the update stage comprises a set of one or more FFs corresponding to each shift register of the shift stage.

10. The invention of claim 8, wherein the PIB further comprises a transfer stage adapted to apply a time-domain transfer to one or more data signals.

11. The invention of claim 10, wherein the DDR, shift, and update stages are adapted to be driven by a first clock signal, and the transfer stage is adapted to be driven by a second clock signal, corresponding to the time domain of the logic core.

12. The invention of claim 1, wherein, to support the output modes, the PIB comprises:

(1) one or more shift registers adapted to multiplex two or more data signals to generate at least one higher-rate data signal; and

(2) a mux adapted to convert two SDR data signals into a single DDR data signal.

13. The invention of claim 12, wherein the PIB further comprises a transfer stage adapted to apply a time-domain transfer to one or more data signals.

14. The invention of claim 13, wherein the shift registers and the mux are adapted to be driven by a first clock signal, and the transfer stage is adapted to be driven by a second clock signal corresponding to the time domain of the logic core.

15. A programmable logic device (PLD), comprising a logic core connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least one PIB can be programmed to perform two or more of:

(a) a double data rate (DDR) input mode in which an incoming DDR data signal is converted into two single data rate (SDR) data signals that are made available to the logic core;

(b) a demux input mode in which an incoming data signal is demultiplexed into two or more lower-rate data signals that are made available to the logic core;

(c) a DDR demux input mode in which an incoming DDR data signal is converted into four or more lower-rate SDR data signals that are made available to the logic core; and

(d) one or more additional input modes in which an incoming data signal is made available to the logic core without any demultiplexing or DDR-to-SDR conversion.

16. A programmable logic device (PLD), comprising a logic core connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least one PIB can be programmed to perform two or more of:

(a) a DDR output mode in which two SDR data signals from the logic core are converted into a single outgoing DDR data signal;

(b) a mux output mode in which two or more data signals from the logic core are multiplexed into a single, higher-rate, outgoing data signal;

(c) a DDR mux output mode in which four or more SDR data signals from the logic core are converted into a single, higher-rate, outgoing DDR data signal; and

(d) one or more additional output modes in which a data signal from the logic core is provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion.

17. A programmable logic device (PLD), comprising a logic core connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least one PIB comprises a transfer stage adapted to apply a time-domain transfer to one or more data signals.

18. The invention of claim 17, wherein the transfer stage is adapted to be driven by a system clock signal, corresponding to the time domain of the logic core.

19. The invention of claim 18, wherein additional circuitry within the at least one PIB is adapted to be driven by another clock signal different from the system clock signal.

20. A programmable logic device (PLD), comprising a logic core connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least one PIB comprises:

double data rate (DDR) circuitry programmable to convert an incoming DDR data signal into two single data rate (SDR) data signals; and

demultiplexing circuitry coupled to the DDR circuitry and programmable to demultiplex each of the two SDR data signals into two or more lower-rate SDR data signals.

21. A programmable logic device (PLD), comprising a logic core connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least one PIB comprises:

multiplexing circuitry programmable to multiplex four or more outgoing single data rate (SDR) data signals into two higher-rate SDR data signals; and

double data rate (DDR) circuitry coupled to the multiplexing circuitry and programmable to convert the two higher-rate SDR data signals into an outgoing DDR data signal.